CLAIMS

1. A bandgap reference voltage circuit comprising:

a modified Brokaw cell including a first transistor and a second transistor, each transistor including a base, an emitter, and a collector; and

a cascode amplifier, wherein collectors of the first and second transistors in the modified Brokaw cell are folded into input terminals of the cascode amplifier.

2. The bandgap reference voltage circuit of Claim 1, wherein an output of the bandgap reference voltage circuit provides a source voltage to the cascode amplifier.

3. The bandgap reference voltage circuit of Claim 2, wherein the first and second transistors comprise lateral PNP transistors.

4. The bandgap reference voltage circuit of Claim 1, further including a stabilizing device for providing loop stability to the cascode amplifier.

5. The bandgap reference voltage circuit of Claim 4, wherein the stabilizing device includes a transistor configured with its source, drain, and substrate coupled to an input voltage source and its gate coupled to the cascode amplifier.

6. The bandgap reference voltage circuit of Claim 4, wherein the stabilizing device includes a capacitive device having one terminal coupled to an input voltage source and another terminal coupled to the cascode amplifier.

7. The bandgap reference voltage circuit of Claim 1, wherein the cascode amplifier includes a bias circuit coupled in operative relation to the Brokaw cell.

8. The bandgap reference voltage circuit of Claim 1, further including an output shunt device coupled to receive an output of the cascode amplifier, wherein the shunt device generates a regulated output of the bandgap reference voltage circuit.

9. The bandgap reference voltage circuit of Claim 1, wherein the modified Brokaw cell and the cascode amplifier are implemented in CMOS technology.

10. The bandgap reference voltage circuit of Claim 1, wherein the first and second transistors include lateral NPN transistors.

11. The bandgap reference voltage circuit of Claim 1, further including one of a resistance and a current source coupled to the output of the bandgap reference voltage circuit.

12. A shunt regulator comprising:

a modified Brokaw cell including a first transistor and a second transistor, each transistor including a base, an emitter, and a collector; and

a cascode amplifier, wherein collectors of the first and second transistors in the modified Brokaw cell are folded into input terminals of the cascode amplifier.

13. The shunt regulator of Claim 12, wherein an output of the bandgap reference voltage circuit provides a source voltage to the cascode amplifier.

14. The shunt regulator of Claim 12, wherein the first and second transistors comprise lateral PNP transistors.

15. The shunt regulator of Claim 12, further including a stabilizing device for providing loop stability to the cascode amplifier.

16. The shunt regulator of Claim 15, wherein the stabilizing device includes a transistor configured with its source, drain, and substrate coupled to an input voltage source and its gate coupled to the cascode amplifier.

17. The shunt regulator of Claim 15, wherein the stabilizing device includes a capacitive device having one terminal coupled to an input voltage source and another terminal coupled to the cascode amplifier.

18. The shunt regulator of Claim 12, wherein the cascode amplifier includes a bias current circuit coupled in operative relation to the Brokaw cell.

19. The shunt regulator of Claim 12, further including an output shunt device coupled to receive an output of the cascode amplifier, wherein the shunt device generates a regulated output of the shunt regulator.

20. The shunt regulator of Claim 12, wherein the modified Brokaw cell and the cascode amplifier are implemented in CMOS technology.

21. The shunt regulator of Claim 12, wherein the first and second transistors include lateral NPN transistors.

22. A cascode amplifier comprising:

a bias current circuit connected to a regulated voltage source;

a first NMOS transistor;

a second NMOS transistor;

a third NMOS transistor; and

a fourth NMOS transistor,

wherein a drain of the first NMOS transistor is connected to a source of the third NMOS transistor and to a first input terminal of the cascode amplifier, a drain of the second NMOS transistor is connected to a source of the fourth NMOS transistor and a second input terminal of the cascode amplifier, and sources of the first and second NMOS transistors are connected to a low voltage source VSS,

wherein substrates of the first, second, third, and fourth NMOS transistors are connected to VSS,

wherein gates of the first, second, third, and fourth NMOS transistors and a drain of the third NMOS transistor are connected to a common node, which is connected to the bias current source, and

wherein a drain of the fourth NMOS transistor is connected to an output terminal of the cascode amplifier.

23. The cascode amplifier of Claim 22, wherein the bias current circuit includes:

a first PMOS transistor;

a second PMOS transistor;

a third PMOS transistor; and

a resistor,

wherein substrates and sources of the first, second, and third PMOS transistors are connected to the regulated voltage source,

wherein the resistor is coupled between VSS and gates of the first, second, and third PMOS transistors, and

wherein a drain of the first PMOS transistor is connected to the resistor, a drain of the second PMOS transistor is connected to the common node, and a drain of the third PMOS transistor is connected to the output terminal of the cascode amplifier.